`default\_nettype none

module mux81(

output logic out,

input logic[7:0] ins,

input logic[2:0] sel

);

logic I0, I1;

mux41 M40(I0, ins[0], ins[1], ins[2], ins[3], sel[0], sel[1]);

mux41 M41(I1, ins[4], ins[5], ins[6], ins[7], sel[0], sel[1]);

mux21 M20(out, I0, I1, sel[2]);

endmodule